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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,534	11/06/2003	James William Kretchmer	134765	8161

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,534	KRETCHMER ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-17 and 20-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-17 and 20-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

7/1/06

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-7, 10-12, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Söderbärg et al. (US 6,063,693).

In re claims 1, 10, Söderbärg et al. teach a method for optical and electrical isolation between adjacent integrated devices, the method comprising:

- forming at least one trench 1 through an exposed surface of a silicon carbide semiconductor wafer 2 (col. 4, lines 1-3) by removing a portion of the semiconductor wafer material 2 (Fig.2a);
- forming an electrically insulating layer 9 (i.e. an oxide) on the sidewalls and the bottom of the at least one trench 1 (Fig.2b);
- filling the at least one trench 1 by conformally depositing an optically isolating material 6 (i.e. a polysilicon, which is an optically isolating material) (Fig.2c); and
- planarizing the semiconductor wafer surface by removing the portion of the optically isolating material 6 above the exposed surface of the semiconductor wafer 2 (Fig.2d).

In re claims 4 and 5, Söderbärg et al. teach forming an electrically insulating layer 9 comprising growing a silicon oxide (col. 3, lines 5-7) on the sidewalls and the bottom of the at least one trench 1.

In re claim 6, Söderbärg et al. teach forming an electrically insulating layer 9 comprising growing or depositing a silicon nitride (col. 3, lines 5-7) on the sidewalls and the bottom of the at least one trench 1.

In re claim 7, Söderbärg teach that the optically isolating material 6 (i.e. polysilicon) comprises an opaque material capable of being deposited conformally.

In re claim 11, Söderbärg et al. teach that the electrically insulating material 9 comprises silicon oxide and the optically isolating material 6 comprises polysilicon, as stated in the rejection against claims 4 and 10.

In re claim 12, Söderbärg et al. inherently teach that the at least trench 1 is located between a plurality of adjacent device sites because the trench is for isolating integrated circuit components from each other (col. 1, lines 8-9).

In re claim 14, Söderbärg et al. teach oxidizing the portion of the optically isolating material 6 (i.e. polysilicon)(col. 5, lines 5-6); and removing the oxidized portion of the optically isolating material (col. 5, lines 22-23).

In re claim 15, Söderbärg et al. teach planarizing the semiconductor wafer by subjecting the portion of the optically isolating material 6 above the exposed surface of the semiconductor wafer 2 to an etching process, i.e. an anisotropic etch process.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8, 9, 17 and 20-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Söderbärg et al. in view of Guo (US 6,894,357).

In re claims 8 and 9, Söderbärg et al. is silent as to the optically isolating material (i.e. polysilicon) being deposited using low pressure chemical vapor deposition (LPCVD) at a temperature below 500 °C.

However, using LPCVD for forming polysilicon has been widely used in the art, as evidenced by Guo (col. 6, lines 10-13 and 25-26), wherein the polysilicon was deposited between 500 and 700 degrees C, which allows slightly below 500 degrees C.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize LPCVD as taught by Guo to form polysilicon in Söderbärg et al, since LPCVD is a good candidate for the foregoing purpose.

In re claim 17, Söderbärg et al. teach a microelectronic device, comprising: one trench 1 in a SiC substrate 2 (col. 4, lines 1-3) and the inside of the trench 1 is coated with an electrically insulating material 9 and filled with an optically isolating material 6 that is conformally deposited.

Söderbärg et al. also suggest that the trench is for isolating integrated circuit components from each other (col. 1, lines 9-10).

Therefore, one of the ordinary skill in the art would have been motivated to apply the teachings of Söderbärg et al. to a situation where two integrated devices are located in a silicon carbide substrate and are physically isolated by the trench, since it is the function of the trench, as suggested by Söderbärg et al. (col. 1, lines 9-10).

In re claim 20, Söderbärg et al. teach that the electrically insulating layer 9 is a thermally grown silicon oxide (col. 3, lines 5-7).

In re claims 21 and 23, Söderbärg et al. is silent as to the optically isolating material (i.e. polysilicon) comprises a low pressure chemical vapor deposition (LPCVD) polysilicon.

However, using LPCVD for forming polysilicon has been widely used in the art, as evidenced by Guo (col. 6, lines 10-13 and 25-26).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize LPCVD as taught by Guo to form polysilicon in Söderbärg et al, since LPCVD is a good candidate for the foregoing purpose.

In re claim 22, Söderbärg et al. teach that the electrically insulating layer 9 comprising a silicon nitride (col. 3, lines 5-7).

In re claim 24 is rejected under Söderbärg et al. in view of Guo, as stated in the rejection against claim 8.

In re claims 25-27, the teachings of Söderbärg et al. are illustrative rather than restrictive. One of the ordinary skill in the art would have been motivated to apply the teachings to any semiconductor devices that need trench isolation to separate semiconductor devices from each other.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Söderbärg et al. in view of Ring (US 2002/0066960).

Söderbärg et al. is silent as to using ICP for etching the silicon carbide (i.e. SiC) wafer.

However, using ICP for etching silicon carbide wafer to form the trench has been widely used in the art, as evidenced by Ring, wherein Ring teaches using ICP for etching SiC substrate 20 (paragraph [0019], [0038] and [0071]).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to use ICP, as taught by Ring, in selectively etching the semiconductor wafer of Söderbärg et al., since ICP is a good means for forming a trench in SiC substrate.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Söderbärg et al. in view of Witek et al. (US 6,146,970).

Söderbärg et al. do not teach using CMP for planarizing the portion of the optically isolating material above the exposed surface of the semiconductor wafer.

However, using CMP for planarizing has been widely used in the art, as taught by Witek et al. (col. 7, lines 33-34 and col. 8, lines 30-32).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to use CMP, as taught by Witek et al., in planarizing the optically isolating material of Söderbärg et al., since CMP is an effective means for planarization.

Response to Arguments

7. Applicant's arguments filed 5/11/2006 have been considered but are moot in view of the new ground(s) of rejection.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (7:30 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hsien-ming Lee
Primary Examiner
Art Unit 2823

July 21, 2006

HSIEN-MING LEE
PRIMARY EXAMINER

7/21/06